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JUNCTION LEAKAGE OF A SiC-BASED NON-VOLATILE RANDOM ACCESS MEMORY (NVRAM)

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ABSTRACT

The potential for developing a one-transistor one-capacitor (1T–1C) nonvolatile random-access memory (NVRAM) on 4H SiC is experimentally investigated in this paper. Using a metal–dielectric–metal (MOM) capacitor as the memory element and a MOSFET on SiC as the select transistor, the charge loss due to the carrier generation, contributing to reverse-biased *pn* junction leakage, can be slowed down to the levels that convert this memory cell into practically nonvolatile. Test metal–oxide–semiconductor (MOS) structures on 4H SiC are used to experimentally determine the time that is needed for the surface generation to create the MOS inversion layer at high temperatures. This relaxation time can then be used to *estimate* the retention time in the NVRAM cell. The calculated charge-retention times for NVRAMs fabricated on n- and p-type substrates are in the orders of 10^{19} s and 10^{18} s, respectively.

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