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GATE DEPLETION ANALYSIS OF PMOSFETS WITH POLYSILICON GATE

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ABSTRACT

This paper presents the study of the polysilicon gate depletion effect (PDE) on the threshold voltage and capacitance of PMOSFETs devices. Simulation analysis over wide range of oxide thickness, gate length width and gate doping were also performed. Simulation results proved that the polysilicon gate depletion effect caused the performance degradation in MOSFET devices due to the reduction of the total gate capacitance as the potential drop of the gate increased. The PDE effect of PMOSFETs with silicon nitride (Si_3N_4) as dielectric material has been proved to have better performance than the PMOSFETs with silicon dioxide (SiO_2) dielectric. It has been found that the polysilicon gate is not compatible to High-K dielectric material.

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